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EXAMINER	
KAO, WEI PO ERIC	
ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/522,057	MA ET AL.	
	Examiner	Art Unit	
	WEI-PO KAO	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 02/27/2008 have been fully considered but they are not persuasive.

In response to the remark on pages 6 and 7:

In response to the entire content of the remarks, in particular that Shiragaki fails to disclose "after high layer processing module detecting the module encounters a problem, it will inform the low layer processing module," examiner respectfully disagrees. According to paragraph [0171], Shiragaki states:

> [0171] **If a failure is detected in multiple layers, the A layer failure detection and recovery processing unit 101 and the B layer failure detection and recovery processing unit 102 are activated simultaneously but individually**, and perform operations up to immediately before switching of a main signal.

In addition, Shiragaki also states the following in figure 3 and paragraph [0182]:

> [0182] At this time, **the layers communicate with each other the fact that failure recovering has started as failure recovery starting notices 203 and 204** using the inter

A-B layer failure recovery information communication terminal and processing units 103 and 104.

In another word, the notices 203 and 204, not only communicate the fact that failure recovering has started on the respective layers, but also indicate the fact that the failure has been detected by the respective layers. Therefore, when the A layer, namely the higher layer, sends the notice 203 to the B layer, namely the lower layer, the B layer is informed with the fact that the higher layer has detected the failure.

In response to the remark on pages 7:

In response to the entire content of the remarks, in particular that Shiragaki reference fails to disclose "a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering," examiner respectfully disagrees. Referring to the figure 3, each layer detects a failure and starts the failure recovery operation simultaneously. Depending on which layer finishes the recovery process first, the layer sends a path reservation notice 207 to the other layer, which has not yet finished the recovery process, to stop the recovery process. Upon receiving the notice 207, the unfinished layer sends a switch authorization notice to the finished layer to notify the finished layer the right to switch/transmit the main signal/data traffic. Considering the example presented by the Shiragaki in paragraph [0185-0188], after the A layer and the B layer have detected the failure and started the recovery processes, the B layer, namely the lower layer, sends the notice 207 to the A layer, namely the higher layer to reserve the path. Upon receiving

the notice 207, the higher layer stops the recovery process (indicating that the higher layer is still experiencing failure) and sends the notice 208 to the lower layer so the lower layer has the right the transmit the data traffic. In another word, the higher layer, which is still encountering a trouble, is isolated and the data traffic is switched by the lower layer, thus bypassing the higher layer.

In response to the remark on pages 8:

In response to the entire content of the remarks, in particular that Chan fails to disclose "high layer processing module extract and insert high layer service of the node from low layer transmission passage, avoiding changing the service between upstream node and downstream node after passing high layer processing module of the said node," examiner respectfully disagrees. First of all, the combination of Shiragaki and Chan et al is reasonable because Shiragaki teaches a general multi-layer communication device with an automatic layer-specific-fault-detection-and-recovery mechanism and Chan et al teach a higher layer, namely ATM, protection mechanism, in which the ATM traffic is traveling on top of a lower layer, namely SONET, communication setup. While it is Chan's objective to provide a robust ATM communication on top of the SONET by protecting the ATM traffic from failures, combining Shiragaki's mechanism is desirable since it provides additional protections. Secondly, it is known it the art the lower layer, namely the SONET, presented in both Shiragaki and Chan's invention provides the high speed physical transmission medium, upon which different communication protocols such as IP or ATM transmits the protocol specific data packets or cells. In addition, since the ATM is the connection oriented protocol, which requires connections and

transmission parameters to be set up prior to the data flow between the source and destination pair (see [0015]), unless the communication path is broken, the connection, transmission parameters and the service the particular connection provides remain unchanged. Further, as indicated by Chan et al in paragraph [0022], the SONET uses the basic data transfer units, namely STS-1/N envelops, to carry the data traffic traveling on top. In order to transfer the data traffic such as ATM for example, ATM cells are encapsulated/put within the STS-1/N envelops. Also note that the process of encapsulation and decapsulation, which is the process of inserting a piece of data such as a packet or cell into another piece of data and extracting a piece of data from another piece of data, has to take place in order for the SONET to transfer the data receiving form the layer above. Therefore, the multi-layer, namely ATM over SONET, communication structure presented by Chan et al exhibits the fact that when an ATM cell is inserted and extracted by a transmission/receiving node and transferred on top of the SONET, the service between its upstream and downstream nodes is not changed after passing through the higher layer; this is especially true when the objective of Chan's invention is to provide a robust ATM communication on top of the SONET by protecting the ATM traffic from failures.

Claim Rejection - 35 USC § 103

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Shiragaki, U.S. Publication No 20020162045 in view of Background of Chan et al, U.S. Publication No 20010046206.

Regarding Claim 1, Shiragaki discloses that **a method for protecting high layer service in the multi-layer communication equipment, comprising the following process** (see Abstract)**: First, low layer processing module provides high processing module with low layer transmission passage** (see Figures 1 and 2, [0004-0006] [0164] [0175] i.e. such multi-layer communication setup is commonly known as IP over SONET/SDH, according to OSI model, SONET/SDH is at physical layer, which provide physical connection between network nodes, IP is at the network layer, which provides routing or logical connection; another common multi-layer setup is ATM over SONET/SDH)**; Third, after high layer processing module detecting the said module encountering the trouble, it will inform low layer processing module** (see Figure 1 Elements 103 and 104, Figure 3 Elements 204/208, [0025] [0030-0033])**; Fourth, a bypass will be set up after low layer processing module detecting high layer processing module encountering the trouble, so as to isolate the high layer processing module encountering the trouble** (see Figures 3 and 4, [0180] [0182] [0185-0188] i.e. according to [0186] layer A remains in the failed state since it is not yet able to recover the failure; according

[0187] layer B is able to finish up the failure recovery and carry out the main signal after receiving the switch authorization notice; in summary a bypass is set up after layer B detects layer A encountering a failure after receiving notice 204 and 208 to carry out the main signal while layer A remains in a failed state). However, Shiragaki does not disclose that **Second, high layer processing module extract and insert high layer service of the said node from low layer transmission passage, avoiding changing the service between upstream node and downstream node after passing high layer processing module of the said node.** Chan et al from the same field of endeavor teach that **Second, high layer processing module extract and insert high layer service of the said node from low layer transmission passage, avoiding changing the service between upstream node and downstream node after passing high layer processing module of the said node** (see [0003] [0006] Line 1-3 [0015] [0017] [0022-0023] i.e. ATM is a connection oriented protocol, which means that a path between the source and destination is set up before data is sent; according to standard OSI operation when such data is sent through the nodes between the source and destination, process of encapsulation and de-encapsulation is performed to not only check VP and VC identifiers to decide the next direction of the path but also reinsert the data into the lower layer payload to deliver the data). At the time of the invention, it would have been obvious to a person ordinary skill in the art to apply the same protection method from Shiragaki to the common ATM over SONET/SDH multi-layer setup. The rationale would have been that since ATM is a protocol commonly used for real time application, which requires much less delay than IP, it is even more desired to have a multi-layer failure protection mechanism for ATM.

Regarding Claim 2, Chan et al further disclose that **a method for protecting high layer service in the multi-layer communication equipment, wherein in the second step, a transparent virtual path connection is set up for the service passing the high layer processing module of the said node, namely for ATM traffic, a cross connection, which changes neither virtual path identification nor virtual channel identification, will be set up, to avoid changing the service between upstream node and downstream after passing high layer processing module of the said node** (see [0015-0016] [0018] [0020] [0022-0023] i.e. according to the OSI model, with the process of encapsulation and de-encapsulation and the help of VPI and VCI, the data is sent from a source node to a destination node through different nodes on a connected path in an ATM network). At the time of the invention, it would have been obvious to a person ordinary skill in the art to apply the same protection method from Shiragaki to the common ATM over SONET/SDH multi-layer setup. The rationale would have been that since ATM is a protocol commonly used for real time application, which requires much less delay than IP, it is even more desired to have a multi-layer failure protection mechanism for ATM.

Regarding Claim 3, Shiragaki further discloses that **a method for protecting high layer service in the multi-layer communication equipment, wherein in the third step, when high layer processing module detects the said module encountering trouble, it will inform low layer processing module by soft messages or hardware signals** (see [0232]).

Regarding Claim 4, Shiragaki further discloses that **a method for protecting high layer service in the multi-layer communication equipment, wherein in the fourth step, said situation that low layer processing module detect high layer processing module encountering trouble further comprising: low layer processing module judges whether the service signal transmitting by high layer processing module is invalid or not, or low layer processing module detects the hardware signals or soft messages sending by high layer processing module indicating its invalidation** (see Figure 3 Element 208, [0186] i.e. once layer B receives the notice 208, it knows that the layer A is not yet recovered from the failure)**.**

Regarding Claim 5, Shiragaki further discloses that **a method for protecting high layer service in the multi-layer communication equipment, wherein said bypass connection is actual connection of the physical lines, or it is logical connection within low layer processing module** (see [0004-0007] i.e. according to OSI model, SONET/SDH is at physical layer)**.**

Conclusion

6. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the

mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WEI-PO KAO whose telephone number is (571)270-3128. The examiner can normally be reached on Monday through Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wei-po Kao/
Examiner, Art Unit 2616

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2616